REMARKS

Applicants gratefully acknowledge Examiner Vicary for taking time from his busy schedule on August 21, 2007, to conduct a telephone interview with co-inventor Gustavson, and Applicants' representative Cooperrider. Applicants believe that the interview was productive and will greatly expedite prosecution. Applicants again remarked how impressed they are by the quality of the evaluation for this application by Examiner Vicary.

Dr. Gustavson provided a summary of how the present invention actually addresses a problem with newer architectures and that the newly-cited articles do not address these newer architectures. Applicants agreed to amend the claims to clarify how the newer architectures are not relevant to the cited articles.

Claims 1-9 and 11-19 are all the claims presently pending in the application. Claims 10 and 20 are canceled.

It is noted that Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-20 stand rejected under non-statutory double patenting over claims 1, 3-6, 8-12, and 14-19 of co-pending application S/N 10/671,937. Claims 1-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claims 1-20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 12-16 stand rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter. Claims 1-20 stand rejected under 35 U.S.C. § 102(b) as anticipated by Gustavson et al.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of executing a linear algebra subroutine on a machine having at least one floating point unit (FPU) with one or more associated load/store units (LSU) to load data into and out of floating point registers (FRegs) of said FPU by way of a cache. For an execution code controlling an operation of the floating point unit (FPU) performing a linear algebra subroutine execution, instructions are inserted to move data into the cache providing data for the FPU so that the LSUs can move the data into the

FRegs in a timely manner for the linear algebra subroutine execution. The data is prefetched into the cache from a memory in a nonstandard format predetermined to reduce a number of data streams for a level 3 processing to be three streams and to allow a multiple loading of loads into the FPU by the LSU, thereby improving an efficiency for the linear algebra subroutine execution

Conventional compilers do not have the capability to automatically pre-fetch (timely move) data into the FPU for Level 3 Dense Linear Algebra Subroutines, particularly in view of the newer architectures having FPUs and LSUs.

The claimed invention, on the other hand, teaches how to timely load data into cache, using a non-standard format predetermined to allow the minimum of three data streams and to allow multiple loading into the FPU. This feature can also be accomplished by conventional compilers, when modified to incorporate the concepts of the present invention.

II. THE DOUBLE PATENT REJECTION

In accordance with the discussion during the telephone interview, Applicants believe that the explanation in the independent claims of the newer architecture, along with the wording that the instruction insertion and data movement relate to pre-fetching of data into cache, provide sufficient basis to distinguish the claims of the present invention from the claims of the cited co-pending applications.

Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE 35 USC §112, FIRST PARAGRAPH, REJECTION

Claims 1-20 stand rejected under 35 U. S.C. §112, first paragraph, as allegedly failing the written description requirement. As best understood from the wording of the rejection, the incorporation into the independent claims of wording for "timely moving" in the context of "pre-fetching" data into the cache, further in view of wording describing the newer architecture and the problems of this newer architecture, should address the Examiner's concerns.

Concerning support in the original specification for the revised independent claims,

the support for newer architecture is found at lines 4-9 of page 11. The support for inserting instructions for moving data is found in lines 1-5 of page 8 and lines 7-9 of page 13. The support for the non-standard format and three data streams is found at line 21 of page 14 through line 12 of page 15.

Concerning the Examiner's concern in paragraph 22 on page 11 of the Office Action, Applicants believe that support for the terminology "Level 3 Dense Linear Algebra Subroutine" is found in various locations in the original specification by realizing that, for example, the term "DGEMM" example beginning on the bottom of page 12 is one example of a level 3 dense linear algebra subroutine, as would be understood by one of ordinary skill in the art.

Concerning the Examiner's concerns in paragraph 34 on page 11 of the Office Action that there is no coverage in the original specification for a compiler modified to incorporate linear algebra theory and techniques as described in claims 10 and 20, these two claims have been canceled to expedite prosecution.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. THE 35 USC §112, SECOND PARAGRAPH, REJECTION

Claims 1, 4, 8, 12, 15, 17, and 18 stand rejected under 35 U.S.C. §112, second paragraph, for use of the terminology "thereby improving an efficiency" or something equivalent. In response, Applicant has amended these claims to eliminate this terminology.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

V. THE REJECTION UNDER 35 U.S.C. §101

Claims 12-16 stand rejected under 35 U.S.C. §101. Applicants have previously amended the language in these claims to indicate "computer-readable storage medium tangibly embodying a program of machine-readable instructions." In paragraphs 44-46 of the latest Office Action, the Examiner required that the specification wording be revised.

Although Applicants do not believe that such specification revision is necessary, the

specification revision above is believed to appropriately address the Examiner's concerns.

Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

VI. THE PRIOR ART REJECTION

The Examiner alleges that the article "Improving performance of linear algebra algorithms for dense matrices, using algorithmic prefetch" by Agarwal, et al., including co-inventor Gustavson, teaches the claimed invention.

In response, as discussed during the above-referenced telephone interview, Applicants believe that incorporation into the independent claims of the description of the newer computer architectures distinguishes from the discussion in this newly-cited reference. As explained during the above-referenced telephone interview, this article by Gustavson et al. was not even considered by the co-inventors as being particularly relevant to the claimed invention because the newer architectures were not covered or addressed in this article and were not a concern in writing this article.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggested by this earlier publication by Gustavson, and the Examiner is respectfully requested to withdraw this rejection.

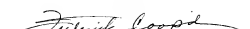
VII. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-9 and 11-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,



Date: September 14, 2007

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CERTIFICATION OF TRANSMISSION

I certify that I transmitted electronically, via EFS, this Amendment under 37 CFR §1.116 to the USPTO on September 14, 2007.

Frederick E. Cooperrider (Reg. No. 36,769)